

FIGURE 1A

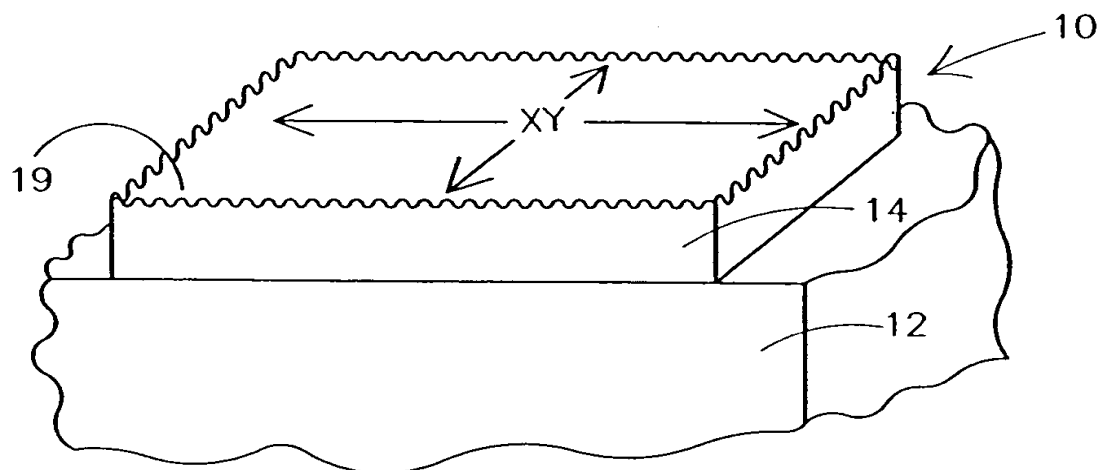


FIGURE 1B

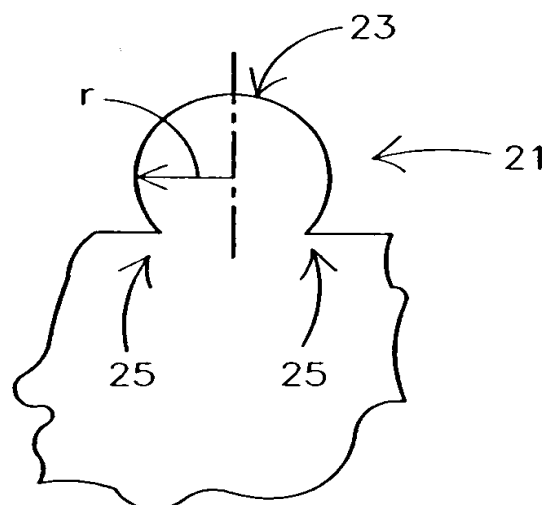


FIGURE 2A

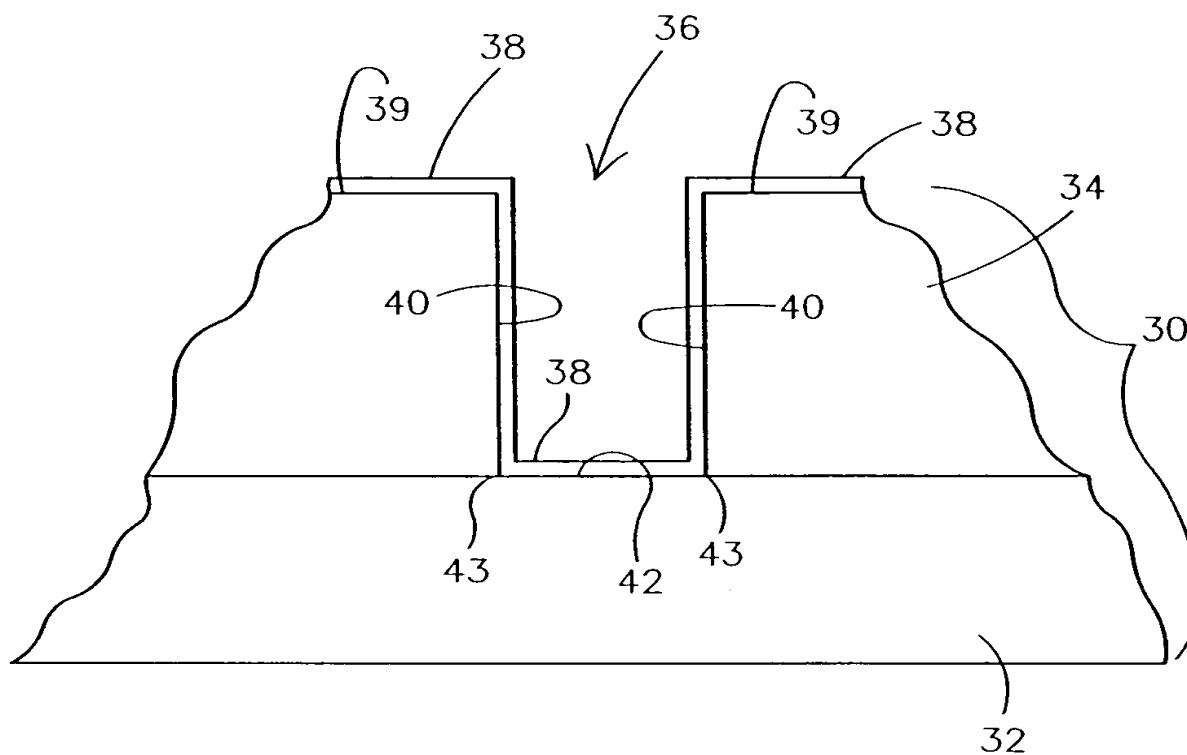
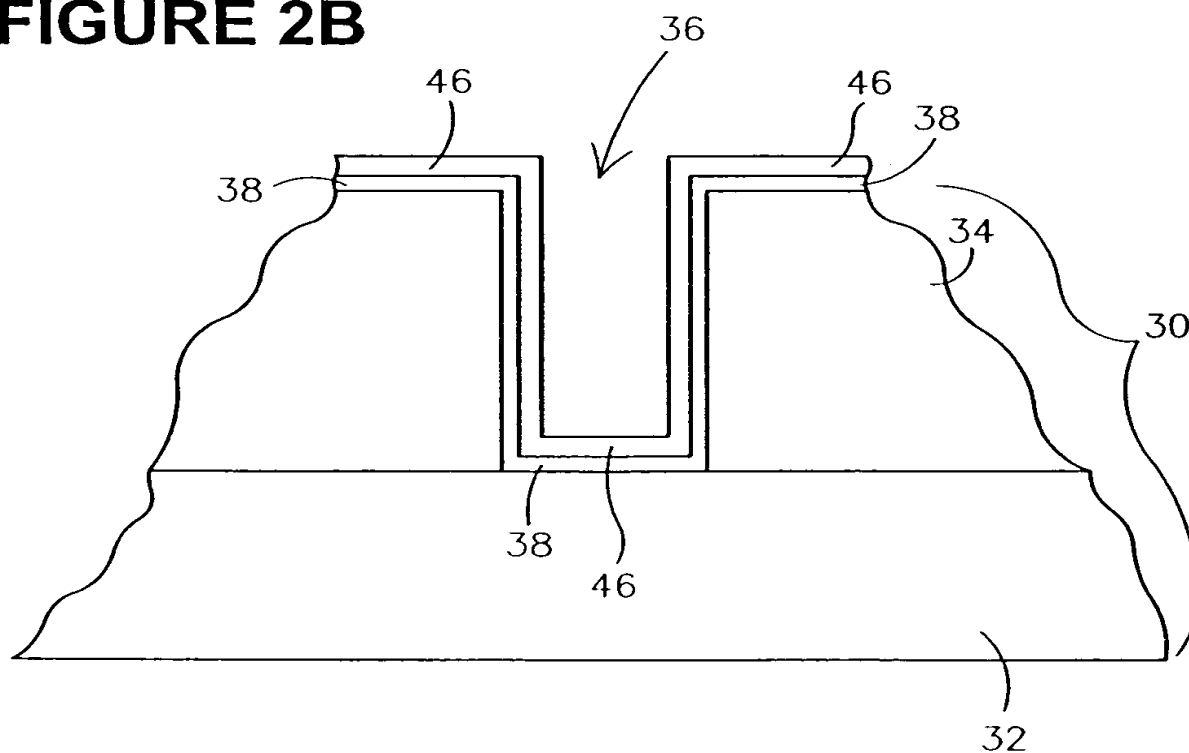
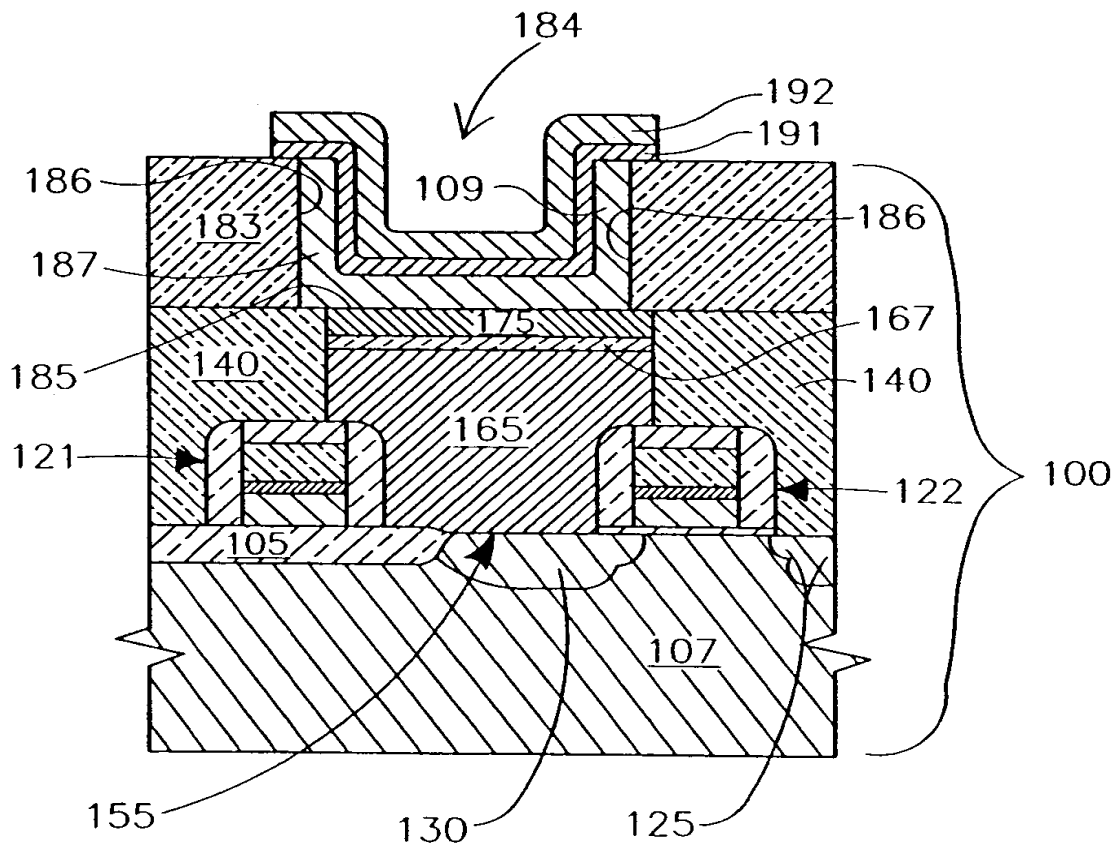


FIGURE 2B



A cross-sectional view of a semiconductor device. A substrate 32 is shown at the bottom. A layer 34 is formed on the substrate. A central well structure is formed in the layer 34, consisting of a central region 36 and two side regions 38. The side regions 38 are separated by a central barrier 33. The side regions 38 are further defined by a layer 46. A top layer 50 is formed on the side regions 38. A top layer 52 is formed on the central barrier 33. A top layer 54 is formed on the top layer 52. A top layer 39 is formed on the side regions 38. A top layer 37 is formed on the central barrier 33. A top layer 30 is formed on the side regions 38.

FIGURE 3



Title: METHODS FOR FORMING ROUGH RUTHENIUM-CONTAINING LAYERS AND
STRUCTURES: METHODS USING SAME

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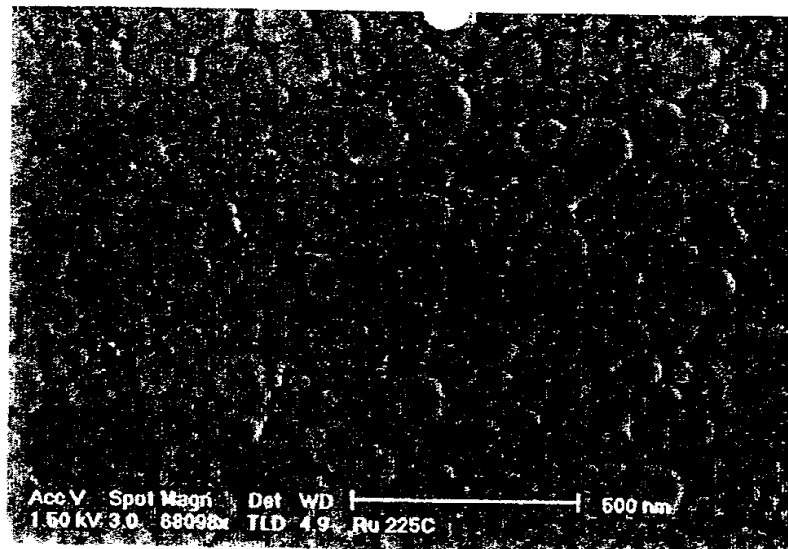


FIGURE 4

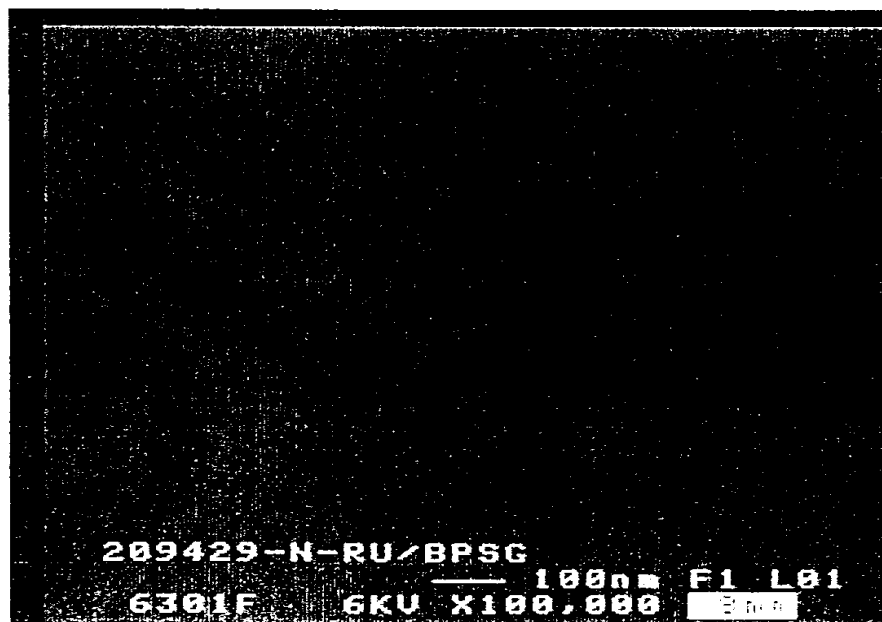


FIGURE 5

FIGURE 6

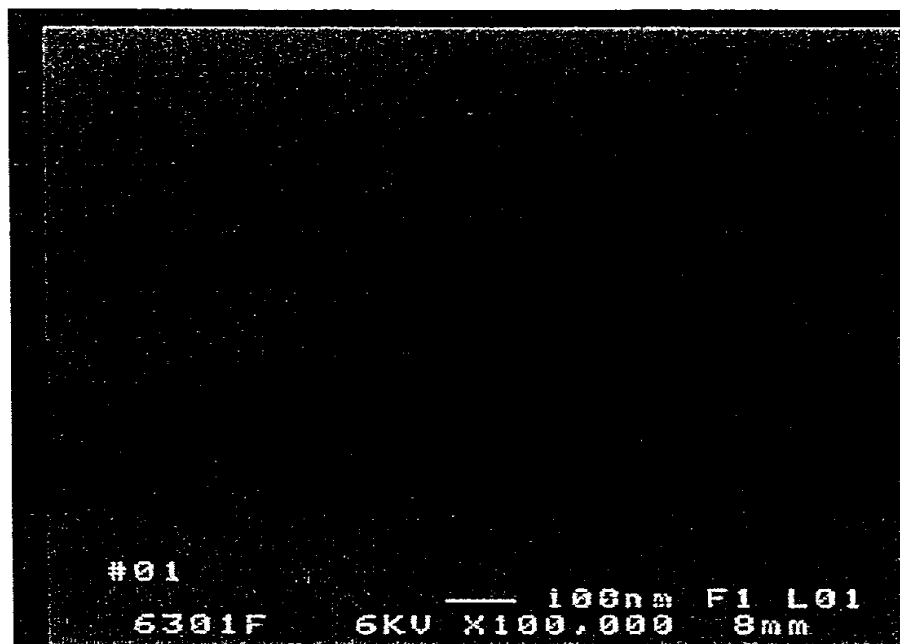


FIGURE 7

